REMARKS

Claims 37-44, 46-50 and 52-60 were pending and rejected. In response, Applicant has amended claims 37, 43-44, 46-50, 52-57 and 59-60. No claim has been additionally cancelled, and no new matter has been introduced. Accordingly, claims 37-44, 46-50 and 52-60 remain pending, and reconsideration is respectfully requested.

In the subject Office Action, the Examiner rejected claims 37-39, 43-44, 46-48, 50 and 52-60 under 35 USC §102(b) as being anticipated by Requa. The Examiner asserted each of the recitations is fully anticipated. In response, Applicant has amended claims 37, 43-44, 46-48, 50, 52-57 and 59-60 to more clearly distinguish the claims over the cited reference.

In particular, claim 37 has been amended to recite:

> "assigning a group of instructions selected from a plurality of groups of instructions partitioned from a program to a subset of interconnected computation nodes preselected from a plurality of interconnected computation nodes;
>
> loading a subset of instructions of the assigned group of instructions into a frame of buffers comprising stores disposed on the subset of interconnected preselected computation nodes having been assigned the group of instructions, prior to the subset of instructions having all necessary associated operands for execution."

Requa teaches a computing apparatus having a Block Processing Section, an Instruction Issue Section, and an Instruction Processing Section. See Fig. 1 of page 427. The Block Processing Section is responsible for dispatching various blocks of instructions to the Instruction Issue Section, and ultimately to the Instruction Processing Section for execution, when the instructions required operands are available. The Block Processing Section is also responsible for processing the instructions of each block, prior to their dispatching to the Instruction Issue Section, transforming the instructions into certain register dependent format suitable for dispatch into the Instruction Issue Section. See e.g. Fig. 6 of page 429. The instructions of the various blocks are comingled and wait in the FIFOs of the Instruction Issue Section, until their associated operands are available. At such time, the instructions are issued from the Instruction Issue section into selected ones of the Scalar, Memory and SIMD Processors of the Instruction Processing Section for exectuion.

In Requa, the Scalar, Memory and SIMD Processors are coupled to the Instruction Issue Section on the input side, and coupled to the Memory System on the output side. The processors themseleves are not "interconnected" to each other, as the term "interconnecting" is understood by those of ordinary skill in the art. See Fig. 1. Further, any one of the Scalar, Memory and SIMD Processors of the Instruction Processing Section may be used to execute any instruction of any block dispatched into the Instruction Issue Section. The processor used depends on the nature of the instruction, i.e. whether the instruction involves e.g., a memory to memory operation, thus needing the Memory Processor, and the processor's availability. Thus, Requa does not teach "assigning a group of instructions selected from a plurality of groups of instructions partitioned from a program to a subset of interconnected computation nodes preselected from a plurality of interconnected computation nodes."

Further, the FIFO holding the instructions as they wait for the availability of their associated operands are located in the Instruction Issue Section. The FIFOs are not part of the processors. Even if we are to assume each of the processors inherently include registers (a point Applicant does not necessary concede), in Requa, each instruction is stored in such registers of one processor, and the instruction is stored into such registers only when its associated operands are available. Thus, Requa does not teach the amended recitation of "loading a subset of instructions of the assigned group of instructions into a frame of buffers comprising stores disposed on the subset of interconnected preselected computation nodes having been assigned the group of instructions, prior to the subset of instructions having all necessary associated operands for execution."

Accordingly, Requa failed to teach at least one reciation of claim 37. So, for at least these reasons, claim 37 is patentable over the cited reference.

Each of claims 47, 57, 59 and 60 include similar recitation or recitations as discussed above for claim 37, and therefore is also patentable over the cited reference for reasons at least similar to the reasons discussed for claim 37.

Claims 38-39, 43-44, 46-48, 50, 52-56 and 58 depend from either claim 37, 47 or 57 incorporating their recitations. Therefore, for at least the same reasons, claims 38-39, 43-44, 46-48, 50, 52-56 and 58 are patentable over the cited reference.

Claims 40-41 were rejected under 35 USC §103 in view of Requa and Official Notice. Without conceding the appropriateness of the Official Notice, since the Official Notice does not remedy the above discussed deficiencies of Requa, claim 37 remains patentable over Requa even in view of the Official Notice. Since claims 40-41 depend from claim 37, therefore, for at least the same reasons, claims 40-41 are patentable over Requa in view of the Official Notice.

Claims 42 and 49 were rejected under 35 USC §103 in view of Requa and Fisher. Since Fisher does not remedy the above discussed deficiencies of Requa, claims 37 and 47 remain patentable over Requa even in view of Fisher. Since claims 42 and 49 depend from claim 37 and 47, respectively, therefore, for at least the same reasons, claims 42 and 40 are patentable over Requa in view of the Fisher.

In view of the foregoing, Applicant submits all pending claims are in condition of allowance. Early issuance of a Notice of Allowance is respectfully requested.

Applicant thanks the Examiner's invitation for an interview. However, for reasons set forth above, Applicant thinks the distinction between Applicant's claims and Requa is pretty clear, thus present the foregoing for reconsideration. Should there be any question with Applicant's response, Applicant likewise invites the Examiner to contact the undersigned at 206-381-8819 (Direct).

Lastly, the Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
Schwabe, Williamson & Wyatt, P.C.

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/Al AuYeung/
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